Modelling HW/SW Co-Designed Processors

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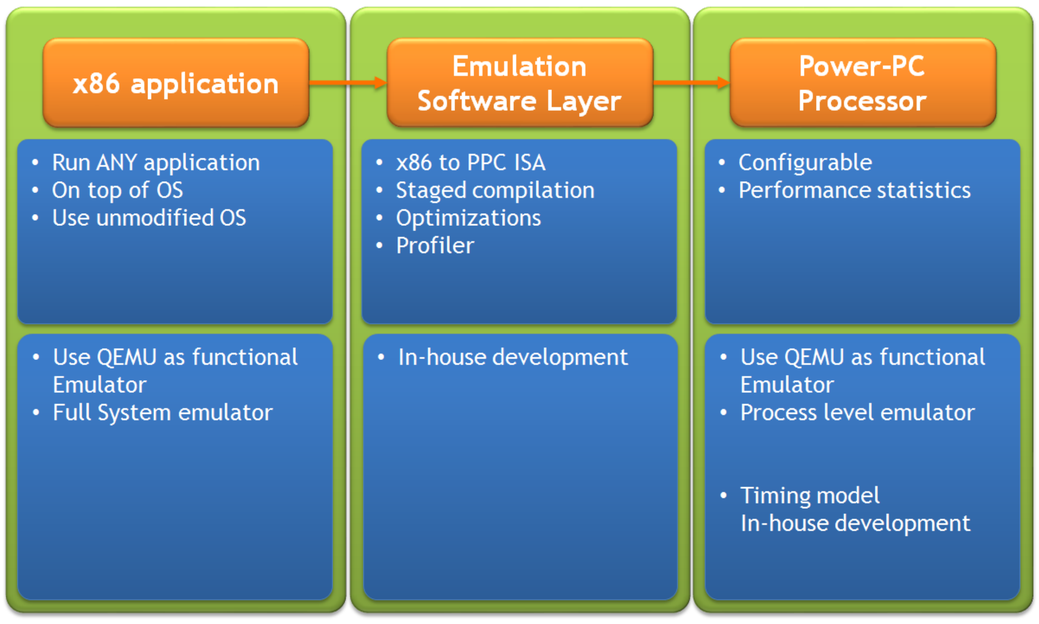
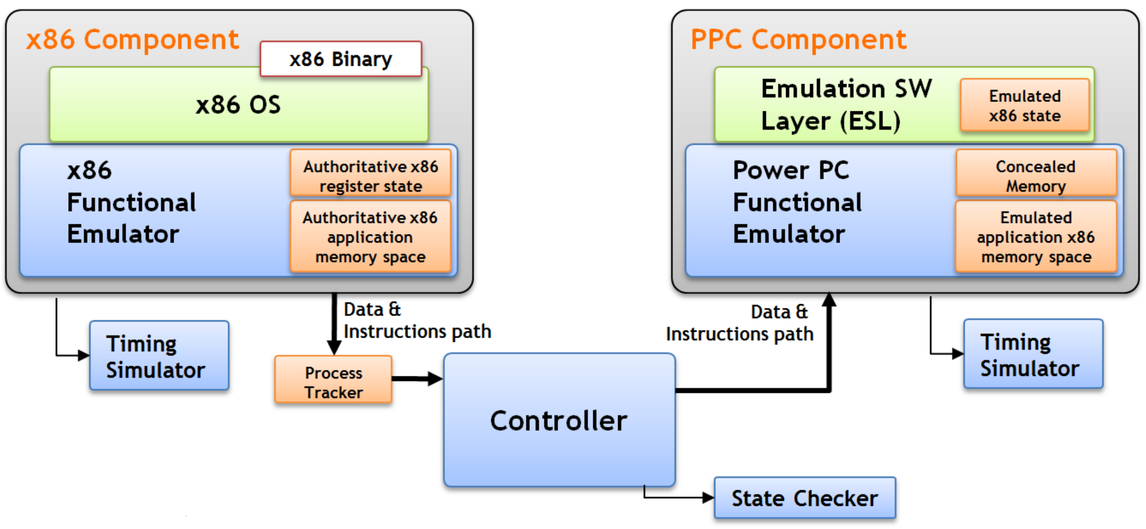
1. Introduction

Hardware/Software co-designed processors have important advantages over traditional hardware-only systems. We propose DARCO, an extensible platform for modelling HW/SW co-designed processors with different guest and host ISAs. Its Emulation Software Layer (ESL) provides staged compilation, which translates and optimizes x86 binaries to run on a PowerPC processor. DARCO also provides timing simulators and a powerful debugging toolchain.

2. DARCO infrastructure

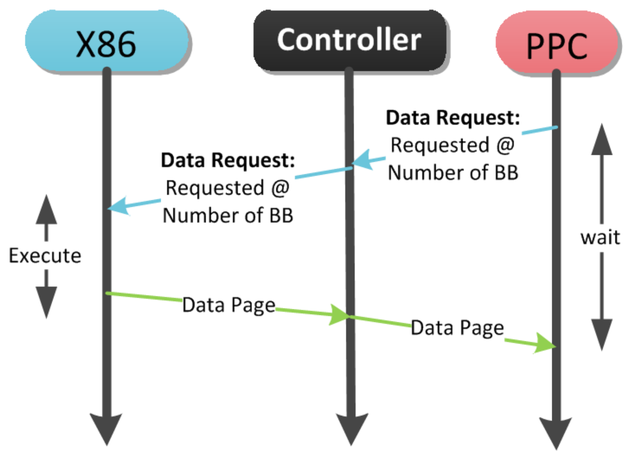


DARCO main components

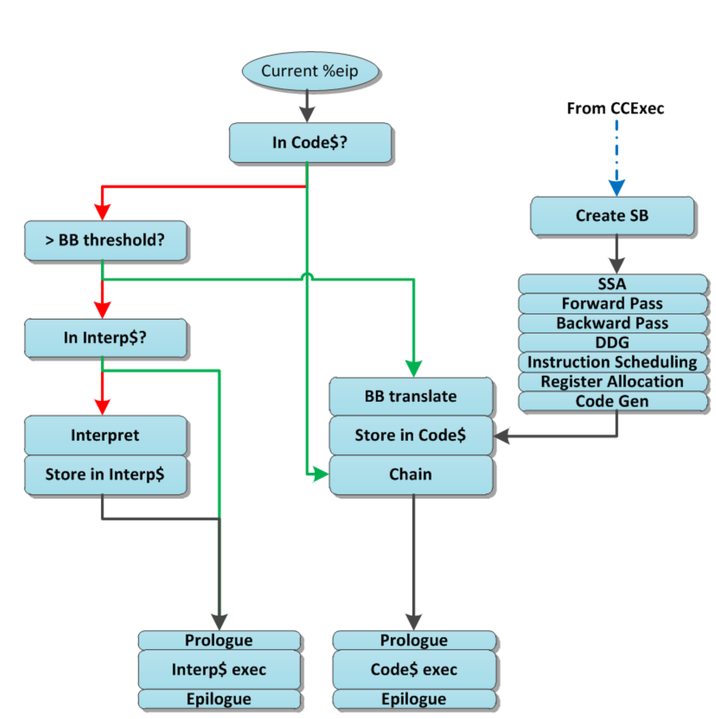


- **x86 Component** : System level QEMU of x86
  Executes the Operating System and the application
- **PPC Component** : Process level QEMU of PPC
  Executes the **Emulation Software Layer**
- **Controller** : Synchronizes execution and handles communication of components
- **Timing Simulator**: In order, multiple issue pipeline

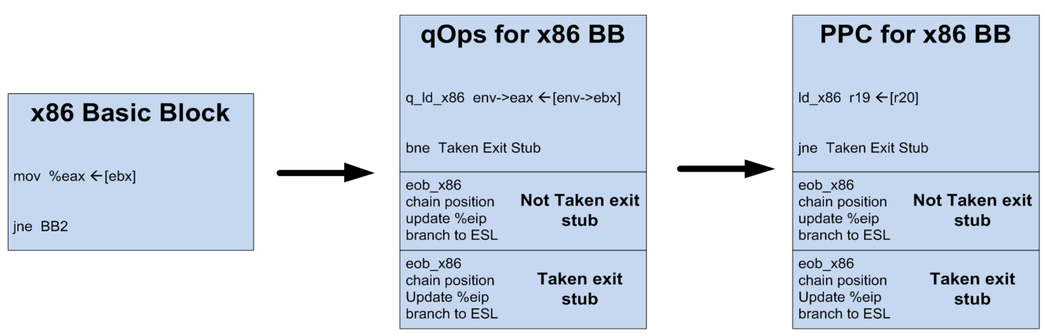
Data page request from the PPC component



Emulation Software Layer execution flow

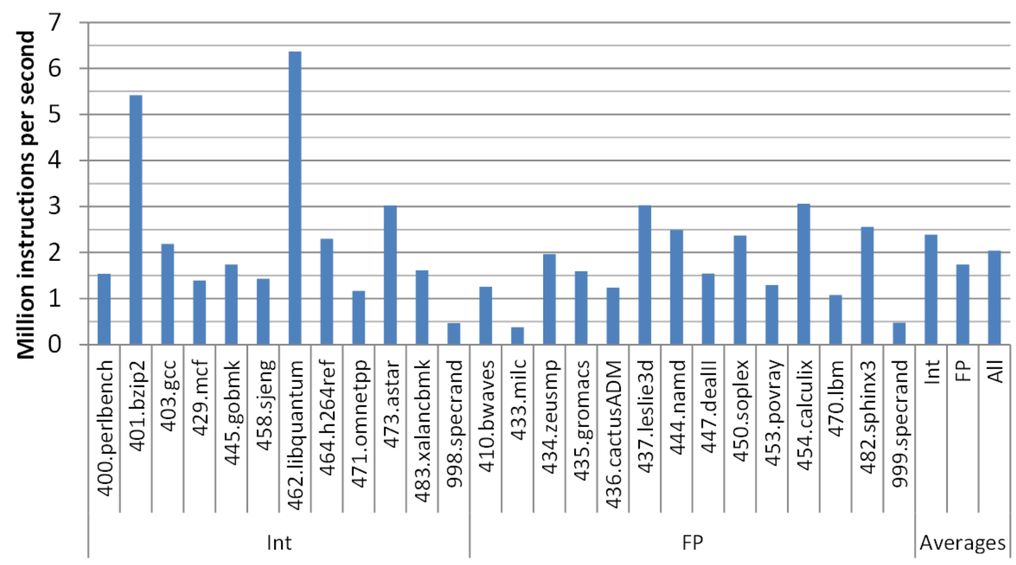


Abstract translation of an x86 BB to PPC



3. Experimental results

We present results about the speed of the infrastructure running SPEC CPU 2006 benchmarks (the first 200 billion instructions). We measure the speed in millions of emulated x86 instructions per second. On average the execution rate of DARCO is approximately 2 million x86 instructions per second using 1 core processors (up to 8 millions on typical dual core machines).



4. Conclusion

DARCO is a complete infrastructure that enables research on HW/SW co-designed processors. DARCO interprets, translates and dynamically optimizes x86 binaries in PPC instructions which execute on top of a functional PPC emulator. Its Emulation Software Layer includes an interpreter, a translator, a scheduler, a register allocator and a staged optimizer. The other key components are the controller that the user interacts with and the timing simulators.

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